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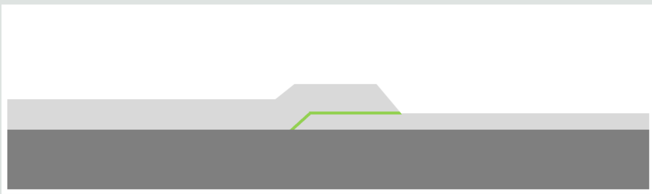
APPLICATION NOTE

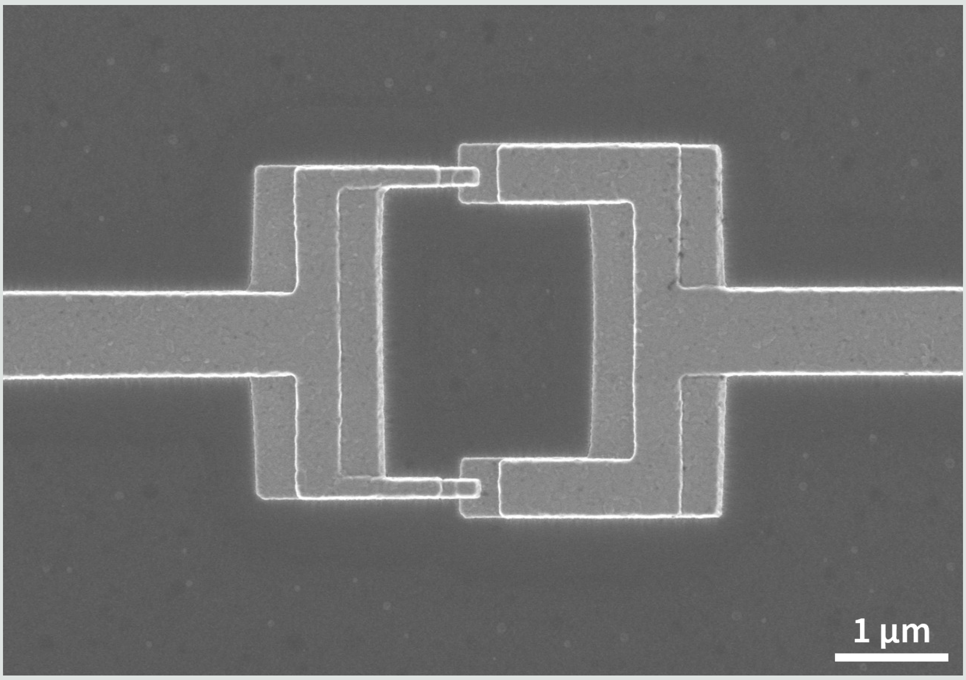
JOSEPHSON JUNCTION DEVICE FABRICATION WITH THE NANOFRAZOR

by

Eliott Clerc

Heidelberg Instruments Nano AG





The NanoFrazor can achieve high-resolution patterning of electrodes and enables reliable fabrication of nanoscale devices. Unlike other nanolithography methods such as e-beam lithography, thermal scanning probe lithography (t-SPL) does not involve a charged beam. These capabilities make the NanoFrazor ideally suited for research and fabrication involving sensitive materials like nanowires and 2D semiconductors, and a powerful tool for nanoelectronics and quantum applications. It can be operated at ambient conditions or integrated into inert atmospheres inside gloveboxes for applications using sensitive materials.

JOSEPHSON JUNCTION FABRICATION OVERVIEW

Josephson junctions (JJs) consist of an overlap of two superconducting materials separated by a weak link. Such devices are enabled by NanoFrazor patterning. In this Application Note, the fabrication of various JJ geometries patterned with the NanoFrazor is demonstrated.

Here, JJ fabrication is enabled by creating an overlap of two aluminum electrodes and forming a thin insulating barrier between the two. The overlap can be made by evaporating metal twice at different angles, with the use of a shadow mask, followed by a bilayer lift-off (BLO) step. The insulating barrier can be formed by an intermediate oxidation step after the first electrode deposition.

Figure 2: Diagram of the Josephson junction fabrication process with the NanoFrazor.

SAMPLE PREPARATION

The sample preparation consists of coating a thick lift-off resist (typically in the hundreds of nanometers) and a top layer of thermally-sensitive resist. The lift-off resist needs to be sufficiently thick to allow overlap of the electrodes after angled shadow evaporation, which forms the junction. This overlap is dependent on the underlayer thickness as well as the angle of evaporation. These can be estimated using trigonometry, such as in the following formula:

- $\Omega = 2y \cdot \tan(\alpha) - \beta$ where Ω is the length of the overlap, y the underlayer thickness, α the angle of evaporation, and β the width of the suspended bridge in the shadow mask

In this application, the following resist layers and recipes were used:

- Silicon substrate: cleaned with acetone and isopropanol (IPA) dips including ultrasonication (30 s each), O_2 plasma treatment (200 W for 1 min), and HMDS pretreatment for adhesion
- Underlayer: LOR-5B spin coated at 4k rpm, nominally 450 nm (baked 170°C for 150 s)
- Thermally-sensitive top layer: PPA 6wt.% spin coated at 6k rpm, nominally 70 nm (baked 110°C for 2 min)

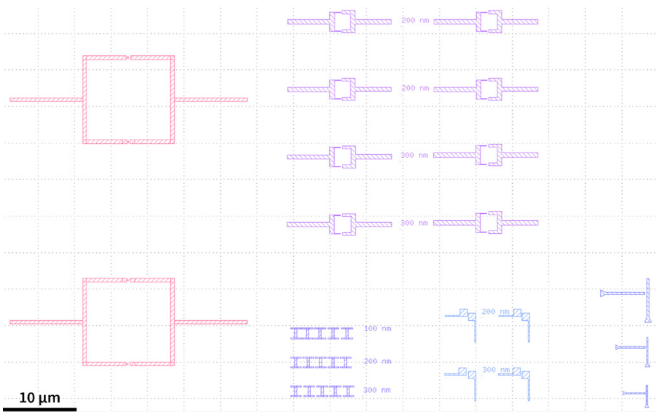


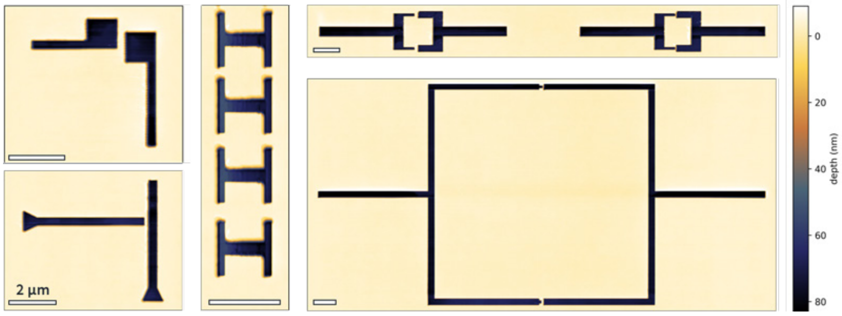
Figure 3: The JJ geometry designs in KLayout.

Figure 1 (Front page): Top: Diagram of a Josephson junction, defined by the overlap of the two electrodes (in green). Bottom: Scanning electron microscopy (SEM) image of a Josephson junction design fabricated using the NanoFrazor. The device consists of an overlap of two aluminum electrodes separated by a thin insulating barrier of a few nanometers of oxide. The bottom electrode is 30 nm thick and the top electrode 80 nm.

NANOFRAZOR PATTERNING AND PATTERN TRANSFER

Various JJ designs were created based on geometries found in literature. The critical dimensions of these designs are the line widths and gap sizes between electrodes, in the range of hundreds of nanometers. The widths of the gaps were calculated according to the underlayer thickness and evaporation angle, and the ideal gaps were determined after the first iteration of samples as being 200 nm to 300 nm.

The Josephson junction designs are patterned with t-SPL in the NanoFrazor. It is essential that the patterns are deep enough to expose the underlayer. The NanoFrazor is capable of reliably patterning down to around 400 nm of depth at this resolution, allowing a thick PPA layer if needed for mechanical stability. In case the underlayer is not exposed during patterning, the remaining PPA resist can be etched away using plasma or reactive ion etching (RIE).



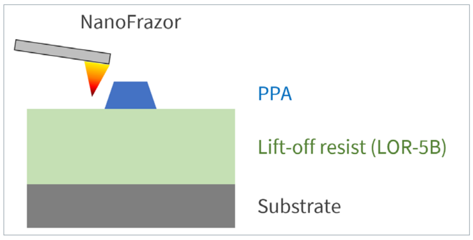
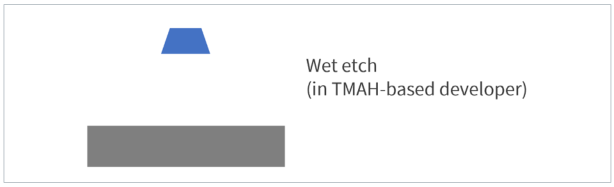


Figure 4: Topography images of the patterns in resist, generated in-situ by the NanoFrazor during patterning. Scalebars are 2 µm.

The underlayer resist is then wet etched. The goal is to etch enough to reach the substrate and create an undercut around the patterned features, without etching so much to risk collapsing the overhanging PPA. It is recommended to test the etch rate of the underlayer material beforehand on a dummy sample. The optimal etch time can then be determined by applying an over-etch factor of around 1.25x to ensure the substrate is reached.

- Example: 500 nm underlayer, 50 nm/s etch rate, 1.25x over-etch factor → $(500\,nm)/(50\,nm/s) \cdot 1.25 = 12.5\,s$

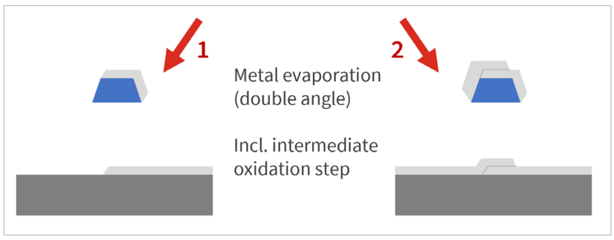


The following wet etching steps and parameters were used:

- Plasma descum: O_2 plasma, 200 W for 5 s
- AZ400K developer (Micro Chemical Corp., diluted 1:4 in DIW) for 8 s
- Rinse in DIW, rinse in IPA (30 s each), dry with N_2

METAL DEPOSITION AND LIFT-OFF

The final critical step in Josephson junction fabrication is the metal deposition. This step defines the junctions by creating an overlap of two metallic electrodes. Aluminum is a common material for Josephson junctions due to its potential as a superconductor and ease of forming a high-quality oxide layer.



Double-angle shadow evaporation is required to create the overlap of the thin electrodes. The angles of evaporation were set to +20° and -20°. This angle proved to be enough to create a significant overlap between the top and bottom electrodes while maintaining good deposition quality. The bottom electrode is 30 nm thick while the top electrode is 80 nm, ensuring conformity of the overlapping layer. An oxidation step at 3 Torr for 3 minutes between the depositions formed the thin insulating barrier of a few nanometers of oxide. A final oxidation at 15 Torr for 5 minutes was done after the depositions.

Following the metal deposition, the remaining resist is lifted off by placing the sample in DMSO at room temperature for about an hour. The process can be assisted by agitating the liquid using a pipette to lift off the metal flakes.

Figure 5 shows the results of the JJ fabrication taken with SEM. The duplicate structures formed by double-angle evaporation are visible, and the small overlap of the electrodes between them define the Josephson junctions.

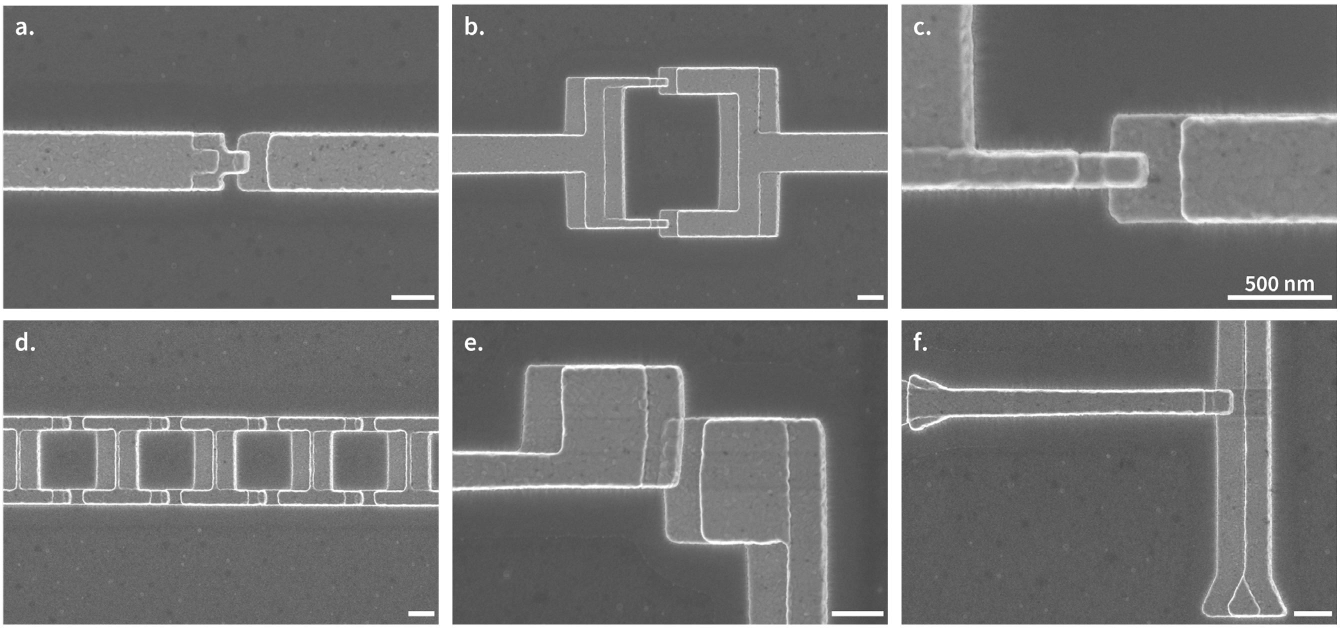


Figure 5: SEM images of the fabricated Josephson junction designs. They consist of an overlap of two aluminum electrodes separated by a thin insulating barrier of a few nanometers of oxide. The bottom electrode is 30 nm thick and the top electrode 80 nm. The image in c. is a close-up of the bottom junction in b. Scalebars are 500 nm.

SUMMARY

The NanoFrazor's high-resolution patterning capabilities enable reliable and straightforward fabrication of Josephson junction geometries. Furthermore, t-SPL enables high quality performance thanks to its damage-free lithography process.

The total time necessary for a round of fabrication such as the application described here is about 5 to 6 hours, including SEM imaging. The NanoFrazor is a reliable and versatile tool that can be integrated in other standardized nanofabrication processes.

Our experienced process and applications engineers continuously develop and improve patterning processes to suit different materials and applications. Often, we do that in close collaboration with our customers. Please feel free to contact us for more details or for a consultation.

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heidelberg-instruments.com

Heidelberg Instruments Nano AG
Bändliweg 30 - 8048 Zürich - Switzerland
Tel.: +41 44 500 3800

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